

10

```
FOR (i=0; i<2; i=i+1)
  begin
    out[i] = 8'b10101010;
    enable[i] = up[2*i];
  end
```

FIGURE 1

```
reg y [3:0];  
WHILE (x <= y) 13  
begin  
    fpl_bit[x+y] = mm_iru[x-y]; 12  
end
```

FIGURE 2

T06050-RT0F5B0

16 18 20 14  
FOR (INIT; EXIT; INC)  
begin 22  
BODY\_OF\_STATEMENTS;  
end

FIGURE 3

FOR (INIT; EXIT; INC)

```
out[0] = 8'b10101010;  
enable[0] = ~up[0];  
  
out[0] = 8'b10101010;  
enable[0] = ~up[2];
```

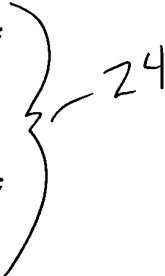


FIGURE 4

T08050-ET0T5860

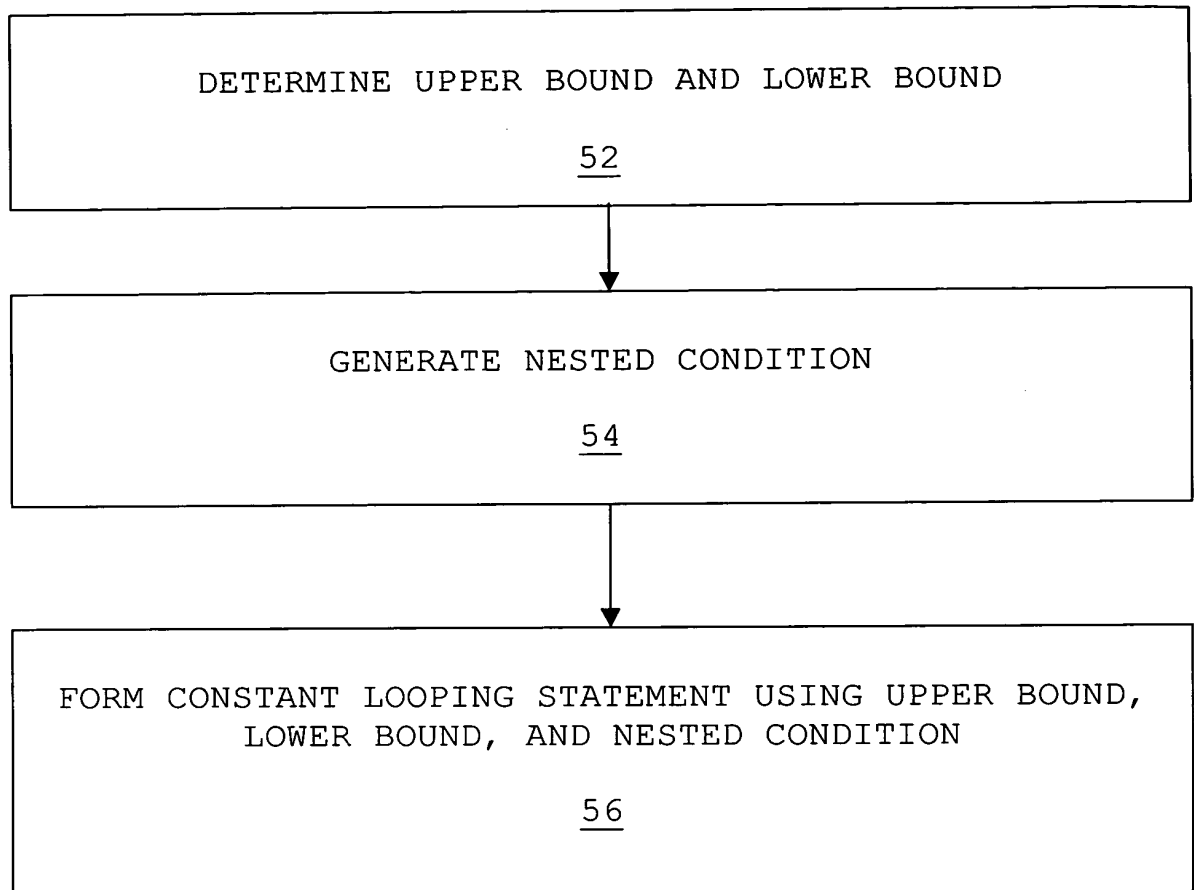


FIGURE 5

FOR (LOWER\_BOUND\_EXPRESSION; UPPER\_BOUND\_EXPRESSION;  
INCREMENT\_EXPRESSION)  
if (INIT && EXIT)  
STATEMENT\_BODY

60 { FOR (LOWER\_BOUND\_EXPRESSION; UPPER\_BOUND\_EXPRESSION;  
INCREMENT\_EXPRESSION) 66  
if (INIT && EXIT) 68  
STATEMENT\_BODY 69

FIGURE 6

80  
82 reg i [3:0];  
84 reg j [1:0];  
reg k [2:0]; 74 76  
{ for (j<=i; i<k; i=i+1)  
70 statement\_body 78  
72

FIGURE 7

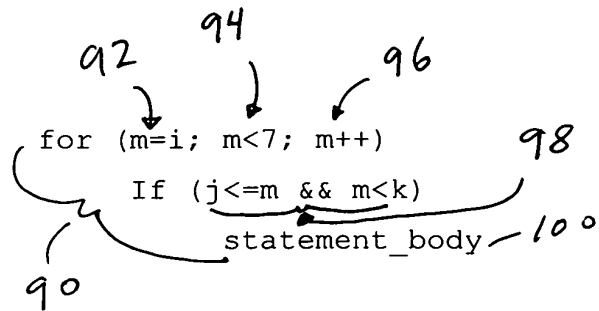


FIGURE 8



```

WHILE ( x <= 15 )
    if ( x <= y )
    begin
        fpl_bit[x+y] = mm_iru[x-y];
    end
end

```

[illegible]

FIGURE 9